SMALL-SIGNAL EQUIVALENT CIRCUIT SCALING PROPERTIES OF AlGaAs/GaAs HBTs

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Abstract

The equivalent circuit model parameters are directly extracted from measured *S*-parameters and then carefully correlated with the device physical layout to provide accurate scaling rules for the design and modeling of HBTs. For devices fabricated with a scaling factor of 4, the predicted *MSG/MAG* is less than 0 5 dB while normalized error in *S*-parameters is less than 10% of measurements for the frequency range of 0 045 to 26 GHz

I. Introduction

In recent years, the heterojunction bipolar transistor (HBT) is emerging as a very promising high-speed device for a wide variety of applications [1]. Small geometries (e g., sub-micron emitter width) and advanced materials (e g , InP-based) have been exploited to improve the frequency responses The scaling design of HBTs has been shown to be more challenging than that of FETs due to the complicated vertical structure, three-dimensional current flow and distributed nature of feedlines [2-3] In this paper, the scaling properties of HBTs will be investigated All intrinsic and parasitic parameters are derived as a function of layout dimensions to analyze the role of device layout design on high-frequency performance of HBTs. The fringing capacitance that limits the ultimate performance of the devices is extrapolated and examined. To validate this approach, the method is applied to devices of scaling factors up to 4 The results showed excellent agreement between the predicted and measured small-signal performance

II. Model Description

The lumped-element small-signal equivalent circuit model of the HBTs used in this work is shown in Fig 1 The model is briefly described as follows The parasitics associated with the probe pads and the device interconnect metals are represented by shunt capacitances (C_{bcp}, C_{bep}, and C_{cep}) and series inductances (L_b, L_e, L_c) The distributed base-collector capacitance is modeled as a combination of the effective intrinsic capacitance, C_c , and the effective extrinsic capacitance, C_{bc} [4] R_{ee} , R_{bb} , and R_{cc} are the emitter, base and collector series resistance, respectively The intrinsic hybrid-π network consists the small-signal input resistance, r_π, the collector output resistance, r_o , the complex intrinsic transconductance, g_m , and the sum of the base-emitter depletion capacitance and the base charging capacitance, denoted by C_π.

III. Approach

A novel parameter extraction technique was previously developed to directly extract the element values from measured *S*-parameters [5] The measured and modeled 2-finger 3×10 μm² HBT is shown in Fig 2 to demonstrate the accuracy This technique typically produced less than 5% normalized error, which is defined as $|S^{mes} - S^{model}|/|S^{mes}|$ averaged over the frequency range, from 0.045 to 26 GHz. The same procedure was applied on devices with varying emitter length to understand the scaling mechanism The extracted model parameters were then analyzed and fit to the geometrical dimensions of the devices

IV. Result and Discussion

The devices used in this study have a fixed emitter width S_E of 3 μm and varying emitter length L_E of 10, 15 and 20 μm. All devices are operated at J_C = 1×10⁴ A/cm² and V_{CE} = 3V with high-frequency measurements performed on-wafer from 45 MHz to 26 GHz

A. Scaling of the Parasitic Resistances and Capacitances

The extracted series resistances R_{ee}, R_{bb} and R_{cc} are found to be inversely proportional to L_E , which is consistent with the results from other work [3]. Fig. 3 illustrates the fit of the extracted emitter resistance to $1/L_E$ The error bars indicates the variations of the extracted resistance over a 3" wafer Excellent fit of the series resistances to $1/L_E$ indicates that the corresponding parameters are correctly described in the equivalent circuit

The scaling of the intrinsic (C_C) and extrinsic (C_{bc}) base-collector capacitances can be analyzed in a similar manner Using a simple parallel plate model of the

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junction capacitance, the base-collector capacitances are shown to scale with the junction area For a given base and emitter width, the intrinsic and extrinsic base-collector capacitances are thus scaled linearly with the base length L_B The fit of the intrinsic and extrinsic base-collector capacitance is shown in Fig 4. It should be pointed out that the extrapolation of zero L_B yields a non-zero capacitance for both C_{bc} and C_C This is a combination of the fringing capacitance and the parasitics which do not scale with the base length In our devices, the fringing capacitance is found to dominate the intrinsic base-collector capacitance and limit the ultimate high-frequency performance of the devices.

B. Scaling of the Intrinsic Elements

The intrinsic transconductance can be easily shown to scale with the collector current due to exponential current and voltage dependence For a given collector current density J_C and emitter width S_E , g_{mo} should thus vary linearly with the emitter length L_E The fitting of g_{mo} is given in Fig 5

Employing the charge control concept, the small-signal input resistance for the base-emitter junction r_π can be represented by

$$r_\pi = \frac{\partial V_{BE}}{\partial I_B} = \frac{\beta_{ac}}{g_{mo}} \quad . \tag{1}$$

Since the incremental common-emitter current gain

$$\beta_{ac} = \frac{\partial I_C}{\partial I_B} = \left[\frac{\partial}{\partial I_C}\left(\frac{I_C}{\beta_{dc}}\right)\right]^{-1} \propto m\cdot(I_C)^{1-\frac{1}{m}} \quad , \tag{2}$$

the input resistance r_π takes the following form

$$r_\pi \propto A(I_C)^B = A(J_C\cdot N_F\cdot S_E\cdot L_E)^B \quad , \tag{3}$$

where N_F is the number of emitter fingers, m is the ideality factor of the base-emitter heterojunction and $A = m(nkT)/q$ and $B = -1/m$. Equation (3) demonstrates the scaling rule for the input resistance. Given that the collector current density J_C and emitter width S_E are kept constant, r_π should vary with the emitter length L_E to the power of $(-1/m)$ as long as T doesn't change. The fitting of r_π is performed in Fig 6 At $J_C = 1\times10^4$ A/cm², since the DC current gain of our device is essentially independent of the collector current, m is approaching unity as depicted in Fig. 6.

In the active forward mode operation of an HBT, the small-signal input capacitance C_π is the sum of the emitter-base junction capacitance and the effective base charging capacitance. This can be written as [4]

$$C_\pi = \frac{\varepsilon\cdot A_E}{x_{de}} + g_{mo}\cdot\tau'_{ec} = L_E\cdot N_F\cdot\left[\frac{\varepsilon\cdot S_E}{x_{de}} + \frac{J_C\cdot S_E}{nkT}\tau'_{ec}\right] \quad , \tag{4}$$

where A_E is the emitter-base junction area, x_{de} is the emitter-base depletion region width and τ'_{ec} is the intrinsic emitter-to-collector transit time. It is clearly seen in equation (4) that the small-signal input capacitance C_π scales linearly with the emitter length L_E when J_C and S_E are kept constant, which is shown in Fig 7 Similarly, the fringing capacitance is obtained as the emitter length approaches zero

V. Validation

The results for a 4-finger 3×10 μm² and 4-finger 3 ×20 μm² , which correspond to a scaling factor of 2 and 4, respectively, are analyzed using this scaling algorithm Fig. 8 shows the predicted and measured performance at $J_C = 1\times10^4$ A/cm² and $V_{CE} = 3$ V for a 4-finger 3×20 μm² device. Throughout the entire 0.045 to 26 GHz frequency range, excellent agreement is observed for both devices. To quantify the modeling result, the predicted *MSG/MAG* is less than 0.5 dB while the normalized error in *S*-parameters is less than 10% of measurements from 0.045 to 26 GHz for both devices Although the experiment uses a scaling factor of 4, we believe that the algorithm should easily apply to devices with scaling factors up to 10.

VI. Conclusion

We have developed the scaling rules for the design of HBTs. This is the first time that the geometrical scaling of the intrinsic parameters of the HBT model has been investigated The described method can provide an expedient and efficient way of evaluating the effects of the epitaxial and layout design to device high-frequency performance. New devices can also be designed and tailored to a specific application with differential changes in the dimension of the unit cell based on this method In addition, the parasitics that limit the device performance, such as the fringing and extrinsic base-collector capacitances in our devices, can be easily identified Although this study uses the AlGaAs/GaAs system, the general principles should apply to other material systems as well

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References

[1] P M. Asbeck, M. F. Chang, J. J. Corcoran, J. F Jensen, R. N Nottenburg, A. Oki, and H. T. Yuan, "HBT application prospects in the US: where and when?," *IEEE GaAs IC Symp. Dig.*, pp. 7-10, 1991.

[2] R. Hajji, F. M Ghannouchi, and A. B Kouki, "Small-signal modeling of high power HBTs using scaling approach", *IEEE MTT-S Digest*, p. 1249, 1994.

[3] U. Schaper, K. H Bachem, M. Karner, and P Zwicknagl, "Scaling of small-signal equivalent circuit elements for GaInP/GaAs hole-barrier bipolar transistors", *IEEE Trans. Electron Devices*, p 222, 1993.

[4] M. B Das, " High-frequency performance limitations of millimeter-wave heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-35, no. 12, pp. 604-614, 1988

[5] Der-woei Wu, D. L. Miller, Mike Fukuda and Yong-Hoon Yun, "Unique determination of AlGaAs/GaAs HBT's small-signal equivalent circuit parameters," *IEEE GaAs IC Symp. Dig.*, pp. 259, 1993.

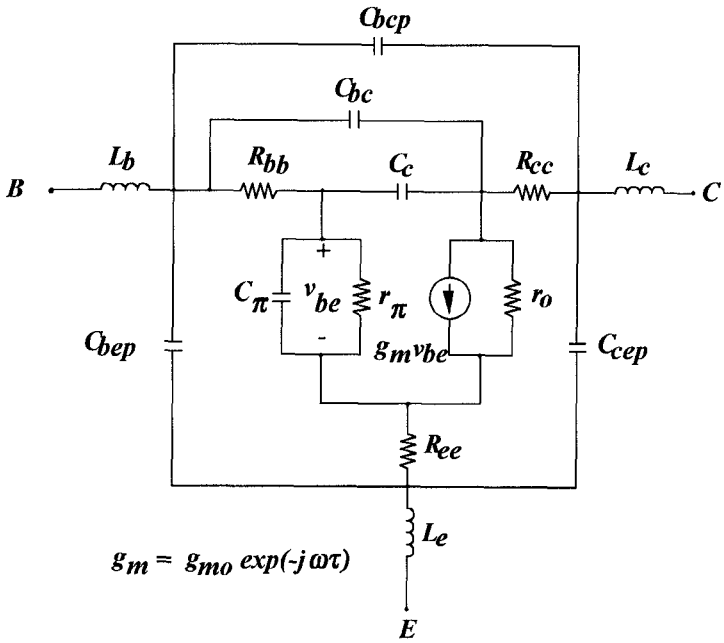

Fig. 1 The lumped-element small-signal equivalent circuit model for HBTs.

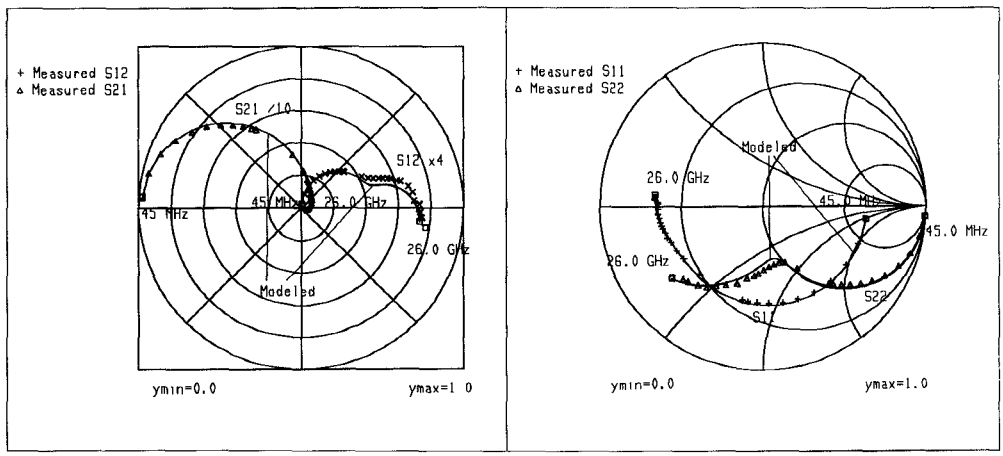

Fig. 2 Comparison between the measured and model-generated S-parameters.

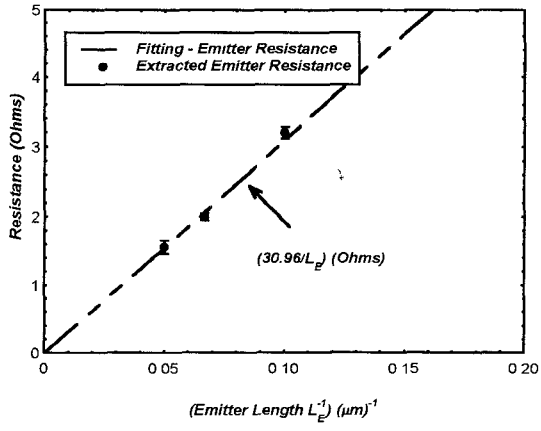

Fig. 3 The fitting of the emitter resistance.

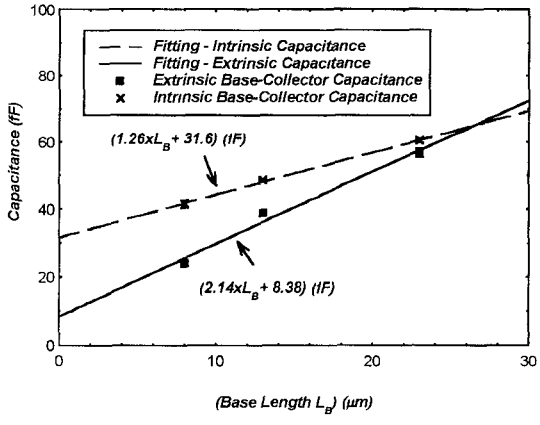

Fig. 4 The fitting of the intrinsic and extrinsic base-collector capacitances.

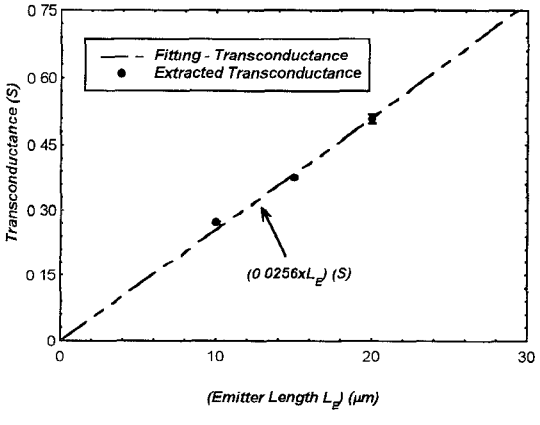

Fig. 5 The fitting of the intrinsic transconductance.

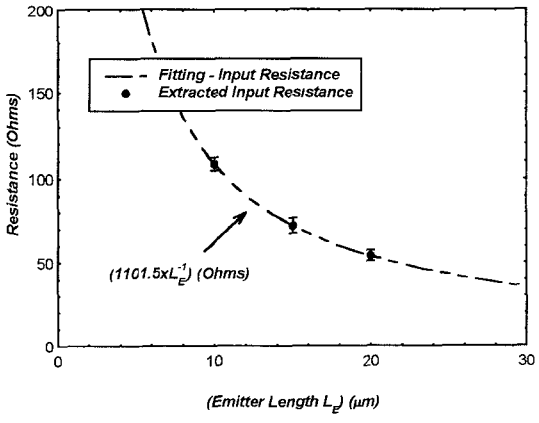

Fig. 6 The fitting of the intrinsic input resistance.

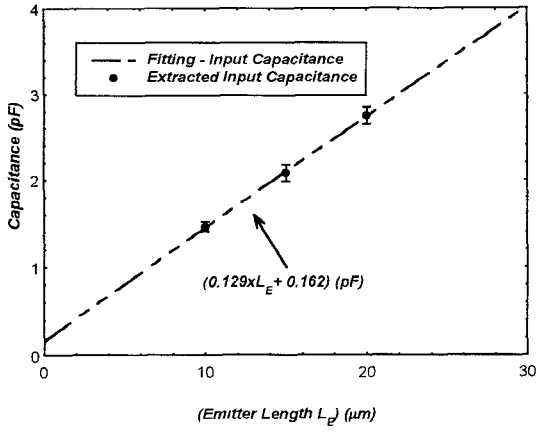

Fig. 7 The fitting of the intrinsic input capacitance.

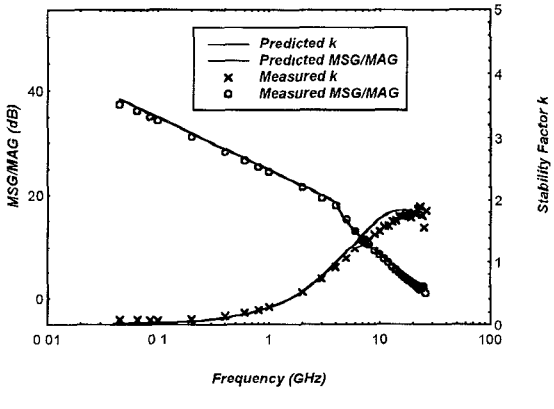

Fig. 8 The predicted and measured Gmax and k for 4-finger 3×20 μm² device.